Microtan

Character Generator Replacement

User Manual

Version 2.0

Contents

Introduction

The Microtan 65 used the National Semiconductors DM8678 or equivalent DM86S64 series character generators as part of its on-board video circuitry. The upper case characters are generated by the xxxxBWF device and the lower case by the xxxxCAE device. The CAE device was an option and so there are a number of Microtans in existence without it fitted, and the device was obsolete many years ago. In TANDOC 2 a design was published by Keith Jones and Tony Kersey to replace these devices with some logic and an EPROM, and this design was adapted for Microtan-R. The Character Generator Replacement board is a development of the original circuit into a plug in replacement that requires no modification to the Microtan.

Design goals and philosophy

In many respects the simplest way to replace an obsolete device is to use a small FPGA, and this approach was considered but discarded in favour of a “historically appropriate” LS TTL design on a through hole board.

The original Jones Kersey design clearly was aiming to reduce the number of new devices and therefore used signals from several places on the Microtan-65 which would have involved several wire links. The goal for this design was to have a direct plug in board that required no modification to the original host and therefore 2 extra devices are needed. Specifically, the original design and Microtan-R use the line counter and address latch from the graphics option, whereas this design creates its own line count and address latch.

The same 2732 as used on Microtan-R was chosen for this design, programmed with the same image, although only ¼ of it is used in normal circumstances. 2732s are obsolete but widely available and generally easier to program than 2716 devices.

The xxxxBWF is still available from specialist obsolete component suppliers and would have been fitted to all Microtans so this board is not expected to be used to emulate an xxxxBWF although it is capable of doing so by custom programming of the EPROM.

The Jones Kersey design actually emulated both the xxxxCAE and the xxxxBWF simultaneously and an option to support this has been included.

Mechanically there seem to be no options to securely mount a small daughterboard on the Microtan so the board is supported entirely by pins plugged into a DIL socket. This is particularly a challenge give the considerable weight of the ceramic EPROM, but is workable for a hobby system that does not move. A standard 16 pin socket is used as a “riser” between the board and the Microtan to lift the rest of the board clear of neighbouring ICs. Other mounting options are possible and are discussed in a further section.

Requirements

A 74LS74 must be fitted in socket L4 on ISS0 Microtan which is E2 on the ISS1 Microtan (recognisable by having a 2716 for TANBUG). This device was part of the original lower case option.

Some older DIP sockets may not accept the turned pins of this board, in which case the Microtan should be replaced, or a different “riser socket” chosen.

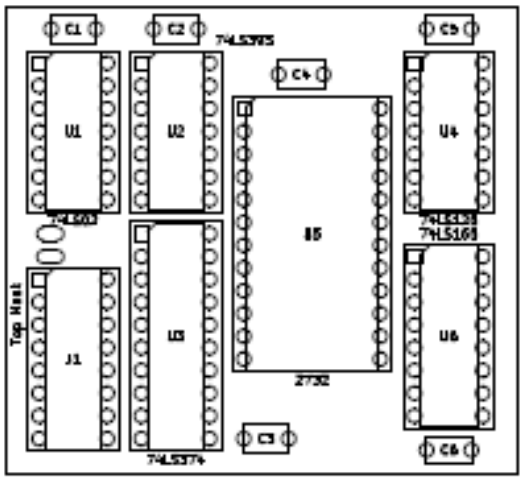
Although the board could be considered a general replacement for the DMs6S64 range of devices it does not emulate pin 7 clock control as this function was not used on the Microtan.

Construction notes

Bill of materials

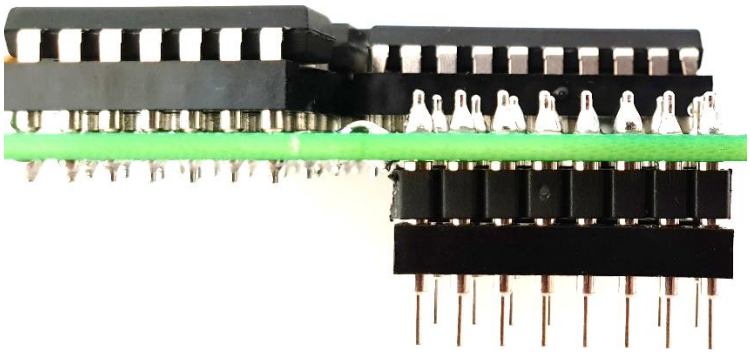
Ident	Description	Qty	Farnell Order code	Notes
J1	2 x 8way turned pin header strip	1	1022217	Part number is a 20 way strip to cut down.
U1	74LS02	1	1740022	
U2	74LS393	1	1740033	
U3	74LS374	1	1739883	
U4	74LS125	1	1470938	
U5	2732A	1		Widely available from specialists or auction sites. Modern programmers cannot program all variants so check before buying.
U6	74LS166	1	1287536	
C1-6	100nF mpc axial capacitor	6	1141777	Lead spacing 5mm (board hole spacing is 5.08mm)
Sockets	14 Way DIP socket 300mils	3	1103845	Part number is for turned pin version
Sockets	16 Way DIP socket 300mils	2	1103846	Part number is for turned pin version note: one of these is to use as a “riser” on J1.
Sockets	20 Way DIP socket 300mils	1	1103848	Part number is for turned pin version
Sockets	24 Way DIP socket 600mils	1	1103851	Part number is for turned pin version
L4 or E2	74LS74	1	1105907	Fit to Microtan
J2	Wire link	1		Offcut from capacitor is ideal

Assembly



Because of its proximity to J1 it is easiest to solder J2 in place first of all.

J1 is soldered on the top of the board and is easier to do before the other components have been fitted. The strips are cut to length and then the smaller pin end should be inserted into the extra 16 pin socket, before inserting the larger pin ends into the board from below and soldering them on the top of the board. This method ensures they are straight and parrallel.

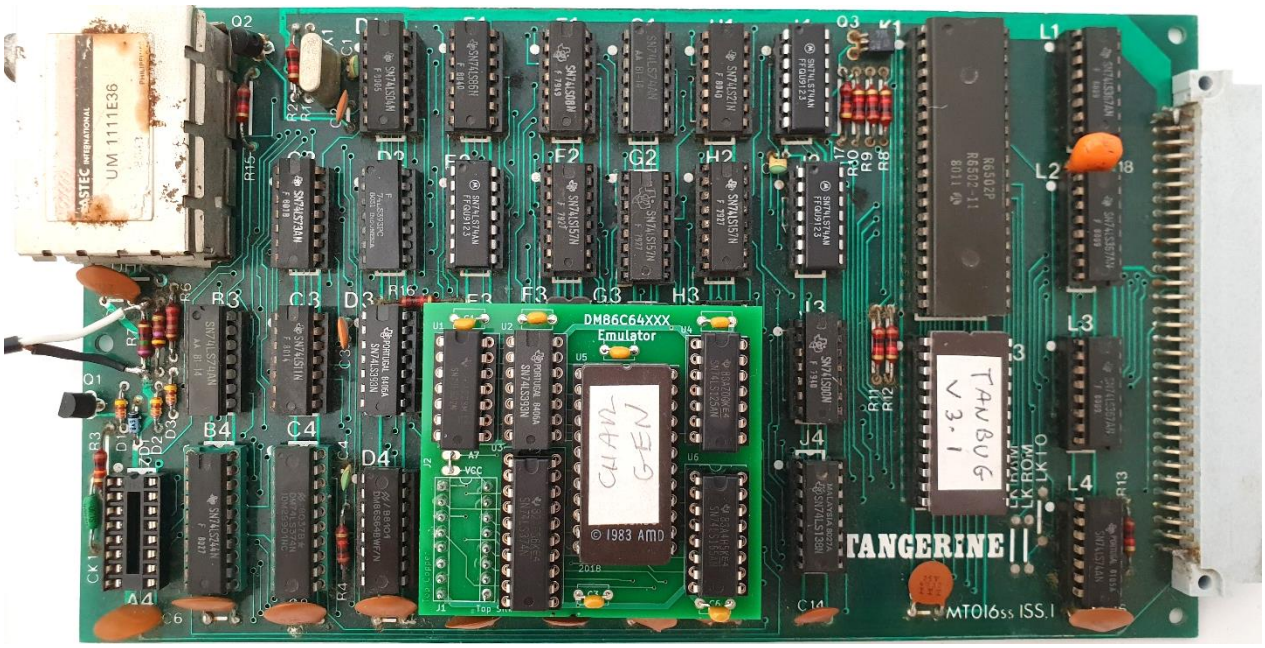


Assembly then continues as any normal PTH PCB in sequence of increasing component height, so fit the sockets first, then the capacitors. Care should be taken with all components to ensure they lie flat to the board. Check for bad solder joints before fitting the ICs.

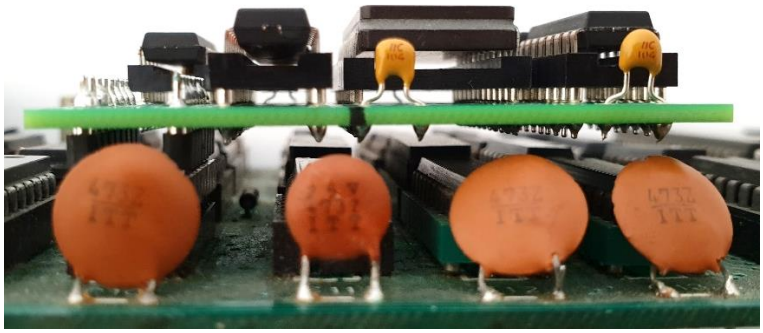
Installation

First fit the 74LS74 to socket L4 on ISS0 Microtan or E2 on the ISS1 Microtan (recognisable by having a 2716 for TANBUG).

To git the board it is usually easiest to remove the 16way socket and fit that to the Microtan in Socket D2 on ISS0 or E4 on ISS 1 then carefully plug the board into the fitted socket.



Check to ensure that nothing is protruding below the board that could cause a short circuit. It may well be prudent to apply some tape. For systems subject to movement double sided foam tape is recommended.



Possible other uses

Remote mounting.

Rather than use pin headers in J1 to make the board a piggy back board it is also possible to use two DIP transition connectors and a length of 16 way ribbon cable. The board itself can then be mechanically located wherever is required. Keep the ribbon cable as short as possible but up to 30cm is likely to work.

Replacing BWF parts

This is currently untested but should work.

When programming the EPROM swap 0x000 to 0x3FF with 0x400 to 0x7FF

Replacing both BWF and CAE parts

This is currently untested but should work.

Remove The 74LS74 from socket L4 on ISS0 Microtan or E2 on the ISS1 Microtan (recognisable by having a 2716 for TANBUG). This ensures that the uppercase character generator output is always selected.

Remove J2 the link between A7 and VCC and connect a wire from the A7 terminal to anywhere the D6 signal is available on the board (Note the DM86CS64xxx identified the character bits as A1 to A7 not D0 to D6 so A7 goes to D6).

Fit the emulator in the Upper case socket C2 on ISS0 Microtan or D4 on the ISS1 Microtan (recognisable by having a 2716 for TANBUG).

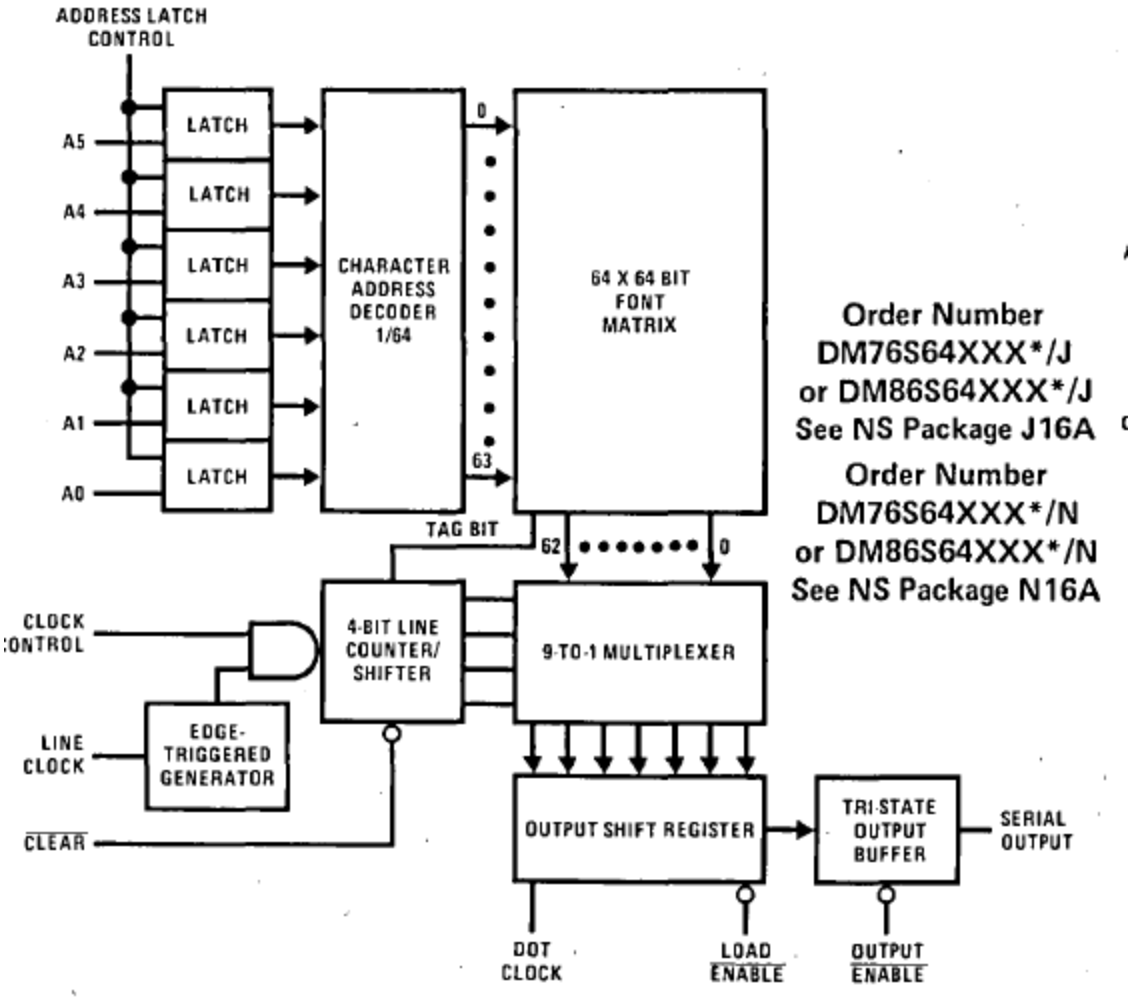
Circuit description.

The following description is provided for interest or education only.

Overview

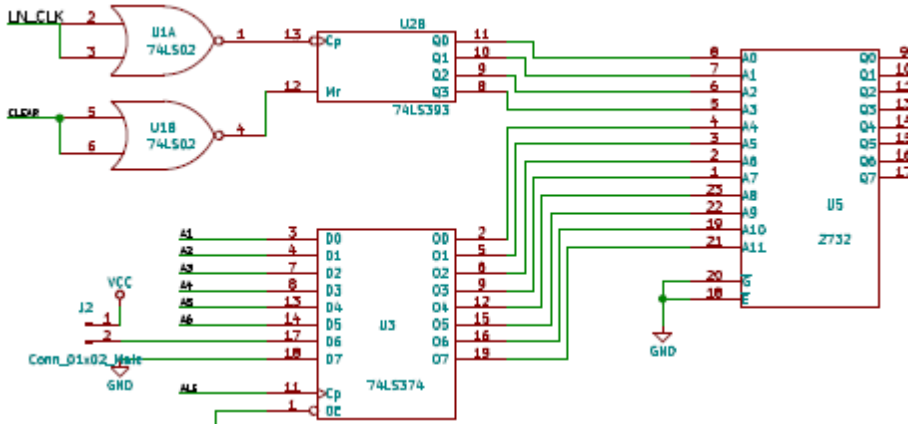
The key function of the character generator is to turn the character value stored in RAM into the dot pattern to display on the screen. The composite video signal scans in left to right lines starting at the top and working down to the bottom. For clarity the characters will be referred to in rows and columns and pattern within in terms of lines and dots. Each character is made up of 9 horizontal lines of 7 dots.

The block diagram of the device can be seen in the datasheet



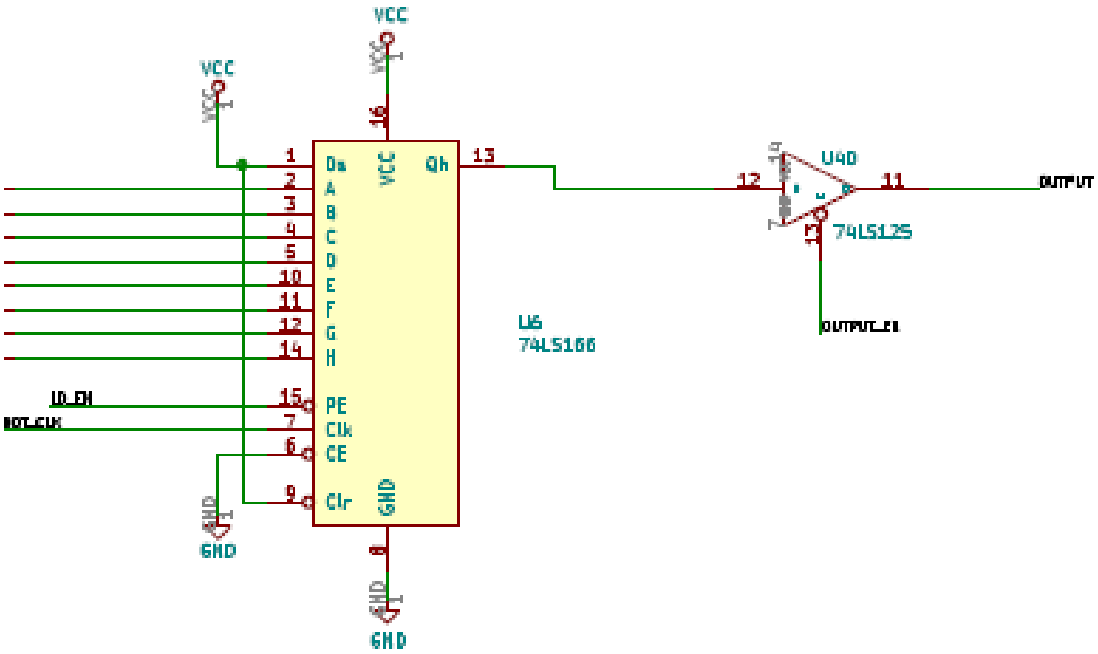
The “Font Matrix” and multiplexor where the dot patterns are stored are replaced by the 2732 EPROM. There is logic to select a line of dots on the left, which is then transferred to a shift register at the bottom and then shifted out.

Line addressing



As the video line is generated from left to right the address to the EPROM is formed from two parts, firstly the video line within the character row. This is derived from the 74LS393 counter, it is incremented at the end of each line, and then reset at the end of each character row. The second part is the character currently displayed in the column being scanned, and this is latched into the 74LS374 by the Microtan. So for one complete line of video the Microtan latches in each character in turn from left to right as the columns are traversed, then the line counter is incremented and the same characters are latched in again for the next line. This happens 9 times until the row is complete, then the line counter is reset and the next row is scanned.

Dot shifting



With the address formed as above the EPROM outputs represent the dot pattern needed to draw one line of dots for the selected character. These are latched into the shift register by LD_EN at the left hand side of each column, and then the DOT_CLK shifts the dots out as the column is scanned from left to right. In the original design, and on version 1 of this board the shift register is a 74LS165

which is an asynchronous load register. A gate was used to ensure the load happens when both LD_EN and CLK are low. This caused a slight timing mismatch the whole thing is running at 6MHz and a dot is only 100ns wide so gate delays are relevant. The timing issue would produce either vertical bars after the character or part dots before. This was less of an issue for both the original board and Microtan-R as all characters are subject to the same timing error, in this plug in board the problem was mainly visible when a lowercase character was followed by an upper case due to mismatch of timing between the emulator and the real part.

The fix in version 2 is to replace the 74LS165 with the synchronous version the 74LS166. This ensures that the load happens exactly on the clock edge and accurately emulates the original device.

Output enable

The Microtan circuit generates the upper case and lower case characters all the time and then the appropriate character generator output is enabled based on the values of D5 and D6 and the graphics bit latched from the RAM into a 74LS74 external to this device. If the graphics bit is set neither generator is enabled.

The response time of a 74LS125 is quite a bit slower than the specification of the original device. To align the timing more accurately a 74F125 could be used, although there are obsolete, they are widely available. This has not been tested.