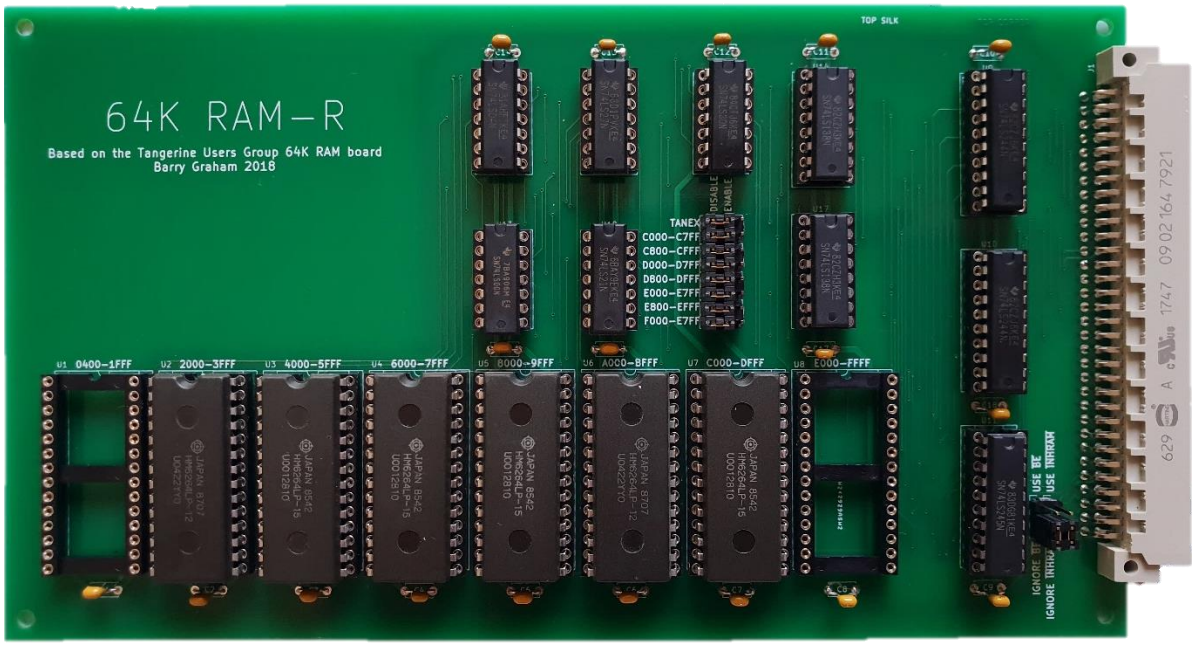
Microtan

64K RAM-R

User Manual



Contents

Introduction

The 64K RAM-R board's main function is to fill the remainder of the Microtan Memory map with RAM. is primarily intended for users who still wish to make use of original Microtan-65 and TANEX boards and require more than 8K of RAM but do not have access to either an original TANRAM or any other memory expansion board. It is not expected to be of use to users with a TANEX-PLUS as this already fills the available address space.

Design goals and philosophy

The board is based on the Tangerine Users Group 64K RAM board and so as well as the main memory it also provides the other two features of that board. Firstly, the ability to overlay any of the TANEX EPROMS such as the BASIC EPROMS with RAM, and secondly the ability to overlay the 7K of RAM provided by 14 x 2114 devices on TANEX should these devices become faulty.

TANRAM and the TUG 64K RAM board both used dynamic RAM, 4116 and 4164 devices, in line with almost all other micros of the era. Other TUG boards used the 6116 2K static RAM device, which again was widely used, but only 16 devices can practically be fitted on the space available on one board. For this board it was decided to use the 6264 8K by 8 Static RAM device for two reasons: Firstly, the 6264 was available as early as 1984 (albeit at a cost of £26, but falling to £3.40 in 1985) and is still in production today. Although he 4164 is widely available it is not still in production. Secondly, DRAM brings significant additional complexity to the circuitry and is relatively difficult to debug for an amateur constructor. SRAM circuitry running at 0.75MHz is relatively easy to fault find.

The address decode and timing circuitry uses 74LS series logic devices, the devices chosen are all still in production and widely available. The resulting board is therefore "historically appropriate" for 1985 whilst using parts in production in 2018 which should be widely available for many years. Through hole devices are used for ease of construction and aesthetics.

The TUG 64K board used DIP switches and pullup resistors, these have been replaced with headers and jumpers to reduce component count and ease construction. The original board had a switch to ignore the I/O decode signal. Use of this switch would appear to create immediate bus contention with devices on TANEX and its purpose is not clear so it has been omitted.

On the original TUG board the decode of the BE signal was such that if the board was not enabled then the TANEX RAM and EPROM overlay were also disabled, meaning that these functions cannot be used in a paged system. This limitation also applies to 64K RAM-R, as additional devices would be needed to overcome it and it is assumed to be an unusual use case.

Requirements

64K RAM-R requires a spare slot in system rack based Microtan system (not the DOS slot if using an original Tangerine motherboard). The original Tangerine Motherboard supported paged memory and the slot used determines which page the board appears as if the BE jumper is set to enable. The board requires at least a Microtan and TANEX. It is expected to work with 6809 systems, although this has not been tested.

The board uses only the +5VDC supply.

The board is intended to work with a TANRAM, TANRAM-R or other board that uses the $\overline{\text{INHRAM}}$ signal. If no such board is fitted and the Motherboard used does not have a pullup for the $\overline{\text{INHRAM}}$ signal then the $\overline{\text{INHRAM}}$ link should be set to disabled.

Construction notes

Bill of materials

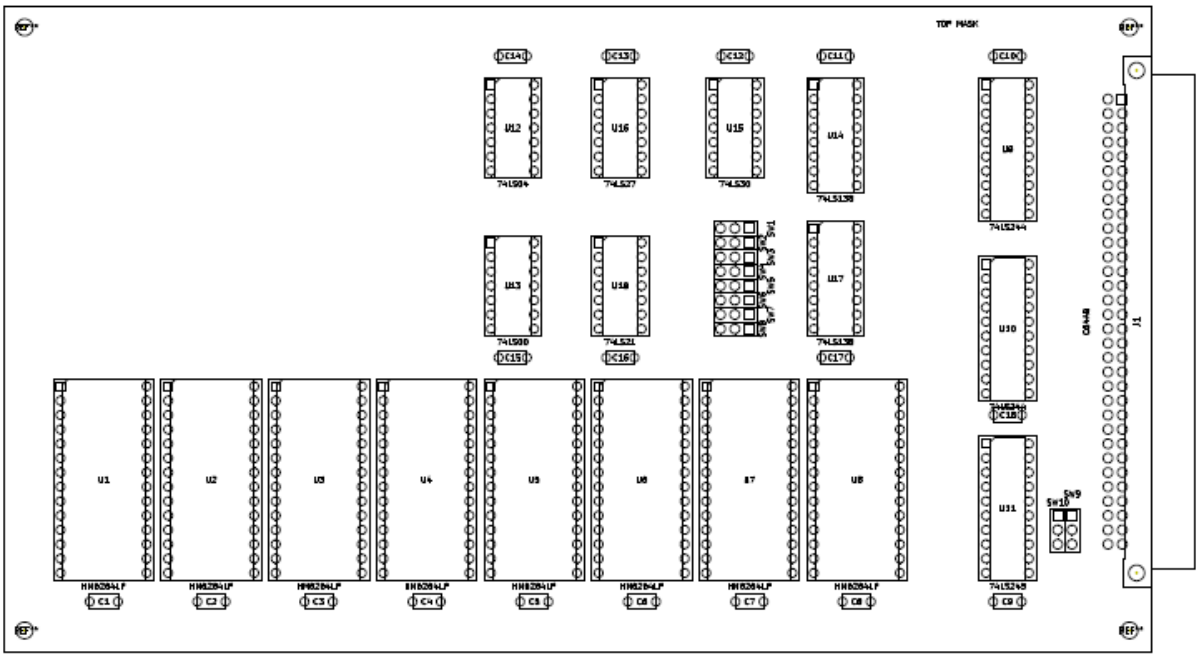
Ident	Description	Qty	Farnell Order code	Notes
J1	DIN 41614 male right angle connector 64 way 2 row a+b	1	1096830	Multiple manufacturers are available
U1-8	6264 8Kx8 Static Ram DIP 600mils	8		Not available from Farnell. See Mouser or ebay. (Take care the 300mils wide device is more common)
U9, U10	74LS244	2	1739688	
U11	74LS245	1	1106085	
U12	74LS04	1	1106072	
U13	74LS00	1	1740021	
U14,17	74LS138	2	1739824	
U15	74LS30	1	1470861	
U16	74LS27	1	1739824	
U18	74LS21	1	1607824	
SW1-10	3 way male pin header 2.54mm pitch	10*	2856507	Part number is for 3x10 to cut into 3x8 and 3x2 only 1 required
C1-18	100nF mpc axial capacitor	18	1141777	Lead spacing 5mm (board hole spacing is 5.08mm)
Sockets	14 Way DIP socket 300mils	5	1103845	Part number is for turned pin version
Sockets	16 Way DIP socket 300mils	2	1103846	Part number is for turned pin version
Sockets	20 Way DIP socket 300mils	3	1103848	Part number is for turned pin version
Sockets	28 Way DIP socket 600mils	8	1103852	Part number is for turned pin version
Jumpers	2 way female jumper	10	2505007	

On the first version of the board the ident for the 6264 devices is incorrect. The correct memory range served by each device is actually as follows

U1	0400-1FFF
U2	8000-9FFF
U3	2000-3FFF
U4	A000-BFFF
U5	4000-5FFF
U6	C000-DFFF
U7	6000-7FFF
U8	E000-FFFF

Notice that if TANEX overlay is not required there is no need to fit U1 and if EPROM overlay is not required there is no need to fit U6 or U8

Construction



As with any PTH PCB it is best to assemble the board in sequence of increasing component height, so fit the sockets first, then the capacitors, then the DIN connector and finally the pin headers for the jumpers. Care should be taken with all components to ensure they lie flat to the board but this is especially critical with the DIN connector. If the mounting screws are used on the connector then they must be tightened before it is soldered.

The part number given for the pin header is for a 3x10 block which can be cut into a 3x8 and 3x2 with a sharp knife. The headers can also be made of smaller strips and in this case it is usually best to use some jumpers to hold them straight and parallel while soldering.

Check for bad solder joints before fitting the ICs.

Installation

Jumper setting.

Memory overlay jumpers.

For operation simply as a replacement for the 48K TANRAM board all the overlay jumpers in the centre of the board should be set to disable. Note that memory overlay will not function in a system using multiple memory boards with paged memory.

To overlay the 7K of RAM provided by 14 x 2114 devices on TANEX these devices MUST be removed from the TANEX board, then the link marked TANEX should be moved to the enable position.

To overlay any of the TANEX EPROMS the EPROM must be removed from the TANEX board and then the jumpers set to enable to relevant 2K blocks of RAM.

EPROM Socket	Typical Use	Jumpers
J2	Basic (2732)	C000-C7FF and C800-CFFF
H2	Basic (2732)	D000-D7FFF and D800-DFFF
D3	Basic (2716)	E000-E7FF
E2	Various	E800-EFFF
G2	XBUG (2716)	F000-F7FF

Bus control jumpers

$\overline{\text{INHRAM}}$: With TANDOS set to USE, without set to IGNORE.

$\overline{\text{INHRAM}}$ (Inhibit RAM) is a signal generated by TANDOS or potentially other boards to disable RAM boards on demand and effectively "carve out" a block of the memory map for the board's own use. In the case of TANRAM it will assert $\overline{\text{INHRAM}}$ whenever its ROM or RAM from A800 to BBFF is accessed. If a board that uses this function is fitted then the link should be set to USE. If no such board is present the INHRAM line may well be floating, and so it is advised to set the jumper to IGNORE.

$\overline{\text{BE}}$: Usually set to IGNORE

$\overline{\text{BE}}$ (Block Enable) is a signal used for the TANBUS paged memory scheme. The original Tangerine motherboard included an additional register to enable one of 7 RAM boards depending on their position in the rack. TANBUG from v2.0 onwards includes routines to support this paged memory. The TUG motherboard and the Microtan-R motherboard do not implement this paging logic. For use in a paged system on an original Tangerine motherboard the $\overline{\text{BE}}$ link should be set to USE, for all other uses is should be set to IGNORE.

Circuit description.

The following description is provided for interest or education only.

Bus buffering

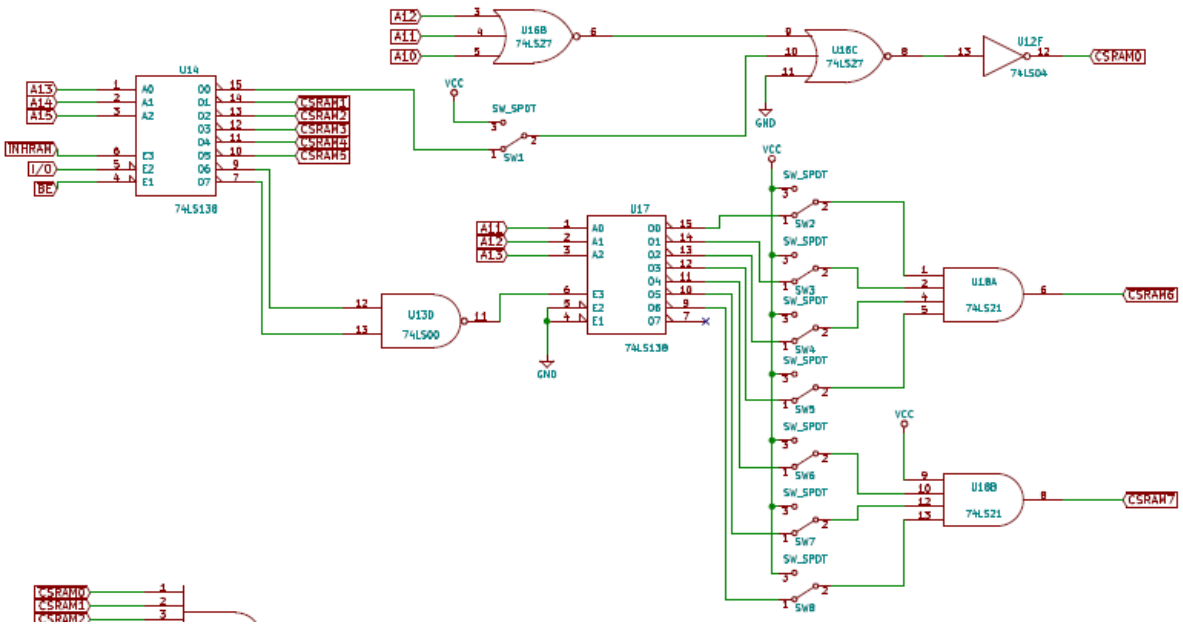
Good practice (and a design requirement in many backplanes) is to only apply 1 standard TTL load to the backplane. $\overline{\text{INHRAM}}$, I/O and $\overline{\text{BE}}$ are only used by a single device and so do not need to be buffered but all other signals do.

For the address bus 2 x 74LS244 Octal buffers (U8 and U10) are used, and as the address bus is unidirectional these are permanently enabled by tying the $\overline{\text{OE}}$ pins to ground. For the data bus a 74LS245 (U11) is used. This requires a direction signal on Pin 1, which is provided by the buffered version of the R / $\overline{\text{W}}$ signal and an enable signal which is provided by the decode logic, the signal is low whenever memory on the board is being accessed to connect it to the bus.

R / $\overline{\text{W}}$ and PHI_02 (the 6502 timing signal) are buffered by double inverting them with gates of a 74LS04 (U12)

Address decode

During the late 1980s and early 1990s it become common practice to use PAL (Programable Array Logic) or later GAL (Generic Array Logic) for memory decode. These devices have many advantages in terms of speed, part count, and programmability. The GAL approach was taken by the designers of TANEX-PLUS due to space constraints and the need for flexibility, however 64K RAM-R has plenty of available board space and GALs are more complex to source and program for hobby constructors so traditional 74LS series logic is used. The circuit is very similar to and inspired by those used on bothTANRAM and the original TUG board.



A 74LS138 (U14) decodes the address space into 8K blocks from A15 to A13. Its outputs are only enabled when $\overline{\text{INHRAM}}$, is high, and I/O and $\overline{\text{BE}}$, are low. For the address space 0x2000 to 0xBFFF the outputs of this device directly feed the $\overline{\text{CS}}$, (chip select) lines of the 8Kx8 RAM devices.

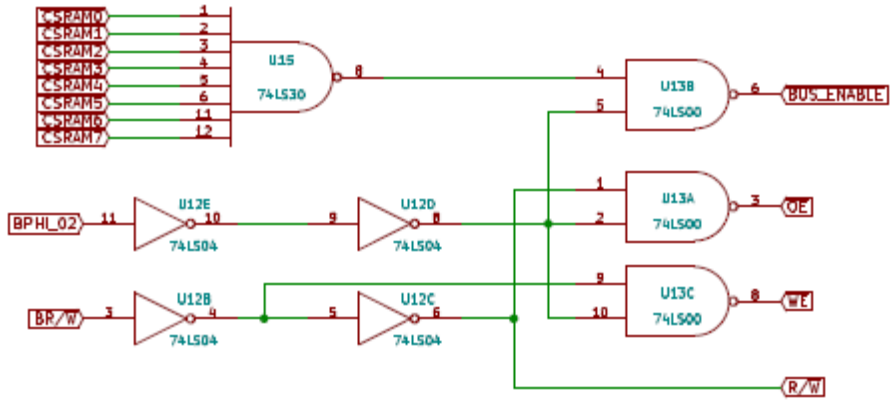
For the TANEX overlay RAM the original TUG board did not overlay the Microtan-65 RAM from 0x0-0x400. This may well be unnecessary as TANEX already isolates this RAM from the bus, however for

consistency this exclusion is implemented with 2 NOR gates from a 74LS27 U16, and a jumper link (shown on the circuit as a switch) is included to disable this entire 8K block.

For the EPROM Overlay the top 2 8K blocks are further decoded into 2K blocks by another 74LS138 (U17). Each of the outputs passes through a jumper link and then 2 AND gates (U16) recombine them into the $\overline{CS}$ lines for 2 more RAM devices.

Timing control

Many designs for low speed memory boards combine the timing and address, the RAM chips are used in what is sometimes called “CS timed” mode. Unlike the 2114 and earlier devices the 6116, 6264 and later devices have separate enable lines so can also be used with the read and write timing implemented separately from the decode. This later mode was chosen due to the relatively long decode cascade.



RAM timing

The $\overline{CS}$ lines are not gated by the phase 2 clock and should be valid and stable before the rising edge of this clock. 2 NAND gates from a 74LS00 (U13) are used to created Output Enable ($\overline{OE}$) and Write Enable ($\overline{WE}$) signals for the RAM chips from PHI_02 and $R / \overline{W}$. The 6264 device does not care about the level of $\overline{OE}$ during a write and in some respects U13A is redundant, however if it were omitted $\overline{OE}$ would be asserted one gate delay before $\overline{OE}$ potentially causing a momentary contention.

Bus transceiver timing

The enable signal for the data bus buffer is created by combining all of the $\overline{CS}$ signals together with a 74LS30 NAND gate, the output of this gate is high whenever any RAM device is selected. This is then gated by the buffered PHI_02 signal from the 6502 which goes high when address data is valid and stable and the read or write should actually take place.

It is worth noting that there is an “inelegance” in the way $\overline{INHRAM}$ is implemented on the original TANDOS that impacts this and all other memory boards designed for TANBUS. TANDOS asserts $\overline{INHRAM}$ 4 gate delays *after* the rising edge of PHI_02 which is 2 gate delays *after* it begins to turn on its own data bus buffer. 64K RAM-R will start to enable the data bus buffer 3 gate delays after the rising edge of PHI_02, and then if $\overline{INHRAM}$ is asserted It will take 3 gate delays to start turning it off. The 74LS245 takes about 4 gate delays to turn on and about 2 gate delays to turn off. So in the case of a read from TANDOS for about 3 gate delays (about 30ns) both TANDOS and 64K RAM-R will be trying to drive the TANBUS databus and will be in contention. It is unlikely that this contention has any practical impact, it is present (and in fact worse) in the original TUG board and Tangerine’s own

TANRAM board, but it is not an ideal design. As $\overline{\text{INHRAM}}$ is functionally an address signal it should ideally be valid and stable before the rising edge of PHI_02 and not gated by it. This observation is in no way intended to criticise any other designer.